IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of | Atty. Docket

MATTHIAS MUTH | PHDE 010023

Serial No.:

Filed: CONCURRENTLY

Title: TRANSCEIVER WITH MEANS FOR ERROR MANAGEMENT

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

4. (Amended) A transceiver as claimed in claim 1, characterized in that the error signal (F) switches a bus transmission stage (5, 6) in the transceiver to the inactive state.

5. (Amended) A transceiver as claimed in claim 1, characterized in that the error signal (F) is signalized to the exterior by means of an error line (ERR), particularly to an application having priority over a protocol controller.

6. (Amended) A transceiver as claimed in claim 1, characterized in that a control line is provided, whose activation resets the means (1) for error management and thus switches the error signal (F) to the inactive state.

7. (Amended) A transceiver as claimed in claim 1, characterized in that the means (1) for error management comprise a flip-flop (14) which, in the set state, supplies the error signal (F).

8. (Amended) A transceiver as claimed in claim 1, characterized in that the means (1) for error management comprise a first AND gate (11) whose output signal is applied to the flip-flop (14) and which sets this flip-flop when the data bus lines (2, 3) are active and when the receiving line (RXD) simultaneously signalizes an inactive bus.

9. (Amended) A transceiver as claimed in claim 2, characterized in that the timer circuit (16) in the means (1) for error management set the flip-flop (14) when the transmission line (TXD) is active for a longer period than a predetermined time interval.

10. (Amended) A transceiver as claimed in claim 1, characterized in that a second AND gate (17) is provided whose inputs receive the reception signal (RXD) and the transmission signal (TXD) and which resets the flip-flop (14)

and thus switches the error signal (F) to an inactive state when the transmission line (TXD) signalizes an active bus and the receiving line (RXD) signalizes an inactive bus.

REMARKS

The foregoing Preliminary Amendment to claims 4-10 was made solely to avoid filing the claims in the multiple dependant form so as to avoid the additional filing fee.

The claims were not amended in order to address issues of patentability and Applicant respectfully reserves all rights she may have under the Doctrine of Equivalents. Applicant furthermore reserves her right to reintroduce subject matter deleted herein at a later time during the prosecution of this application or continuing applications.

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Respectfully submitted,

By ____________________
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APPENDIX

4. (Amended) A transceiver as claimed in claim 1 ~~or 2~~, characterized in that the error signal (F) switches a bus transmission stage (5, 6) in the transceiver to the inactive state.

5. (Amended) A transceiver as claimed in claim 1 ~~or 2~~, characterized in that the error signal (F) is signalized to the exterior by means of an error line (ERR), particularly to an application having priority over a protocol controller.

6. (Amended) A transceiver as claimed in claim 1 ~~or 2~~, characterized in that a control line is provided, whose activation resets the means (1) for error management and thus switches the error signal (F) to the inactive state.

7. (Amended) A transceiver as claimed in claim~~s~~ 1 ~~and 2~~, characterized in that the means (1) for error management comprise a flip-flop (14) which, in the set state, supplies the error signal (F).

8. (Amended) A transceiver as claimed in claim~~s~~ 1 ~~and 7~~, characterized in that the means (1) for error management comprise a first AND gate (11) whose output signal is applied to the flip-flop (14) and which sets this flip-flop when the data bus lines (2, 3) are active and when the receiving line (RXD) simultaneously signalizes an inactive bus.

9. (Amended) A transceiver as claimed in claim~~s~~ 2 ~~and 7~~, characterized in that the timer circuit (16) in the means (1) for error management set the flip-flop (14) when the transmission line (TXD) is active for a longer period than a predetermined time interval.

10. <u>(Amended)</u> A transceiver as claimed in claim~~s~~ 1, ~~2 and 7,~~ characterized in that a second AND gate (17) is provided whose inputs receive the reception signal (RXD) and the transmission signal (TXD) and which resets the flip-flop (14) and thus switches the error signal (F) to an inactive state when the transmission line (TXD) signalizes an active bus and the receiving line (RXD) signalizes an inactive bus.

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